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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

VERIGY US, INC, a Delaware Corporation Plaintiff, vs. ROMI OMAR MAYDER, an individual, WESLEY MAYDER, an individual, SILICON TEST SYSTEMS, INC. a California Corporation, SILICON TEST SOLUTIONS, LLC, a California Limited Liability Corporation, inclusive, Defendants.	**Civil Case No.: C07-04330 RMW (HRL)** **DECLARATION OF DR. RICHARD BLANCHARD** Date: November 9, 2007 Time: N/A Dept.: Judge: Hon. Judge Whyte

[redacted]

DOCUMENT SUBMITTED UNDER SEAL

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Expert Witness Declaration

Dr. Richard Blanchard

I. Introduction

a. The Question Posed

1. I, Dr. Richard A. Blanchard, have been asked by Silicon Test Systems ("STS") to provide opinions and technical information concerning the development of the "Flash Enhancer" integrated circuit and its incorporation on probe cards used to test specific types of memory chips.
2. It is my understanding that Verigy, the previous employer of Romi Omar Mayder (the president of STS), alleges that the integrated circuit, known as the "Flash Enhancer" was developed using proprietary Verigy information and technology. In addition, Verigy alleges that Mr. Mayder has sent documents containing trade secrets to third parties not under a confidential disclosure agreement. My specific assignment is to determine:
   a. Whether the Verigy project code named [redacted] is functionally equivalent to the [redacted]
   b. Whether the information contained in the exhibits attached to the [redacted] are publicly available, or well known in the semiconductor test industry. These documents will be referred to as:
      i. [redacted]

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vi. [redacted]

c. Whether the information contained in [redacted] is publicly available, or well known in the semiconductor test industry. This document will be referred to as the [redacted]

d. Whether the information contained in the [redacted] is publicly available, or well known in the semiconductor test industry.

e. Whether the existing [redacted] origins derive from any of these sources. If so, to what degree.

f. Whether the '[redacted] integrated circuit being [redacted] was developed using only publicly available information (and/or customer provided information) or whether proprietary Verigy information was used.

My analysis, opinions, and reasoning are detailed below.

3. This report is based on information currently available to me. If new information becomes available to me, I expressly reserve the right to expand or modify my opinions as my investigation and study continue.

b. Executive Summary of Conclusions and Considerations

4. Summary of Conclusions: I conclude that:

a. [redacted] is not derived from any of the documents outlined in section (a) above.

b. [redacted] custom integrated circuit that that has been [redacted]

c. [redacted]

d. Each of the documents discussed in section (a) above is based on information publicly available or known in the industry. Most notably, there are several patents that disclose the use of switches (or similar) on probe cards to increase the efficiency of the

semiconductor test process. [redacted]

5. Summary of Information Considered:

a. The conclusions of paragraph 4 were reached after review of (1) relevant patents and patent applications, (2) [redacted], (5) Honeywell publicly available data sheets, and (6) other publicly available sources.

c. My Qualifications

6. My qualifications to testify on this matter are set forth in my curriculum vitae, which is attached as Exhibit A. My resume includes both my educational background and work history. I have also summarized some of my experience below.

7. I received BSEE and MSEE degrees, respectively, from the Massachusetts Institute of Technology in 1968 and 1970, and a Ph.D. degree from Stanford University in 1982, also in electrical engineering. I am a member of a number of professional organizations including IEEE (Institute of Electrical and Electronics Engineers) and IMAPS (International Microelectronics and Packaging Society).

8. I have worked in or consulted for the semiconductor industry for nearly 40 years as an electrical engineer. Projects that I have worked on or managed include the development of discrete devices, the development of integrated circuits, semiconductor device and integrated circuit manufacture and the assembly of semiconductor devices and integrated circuits.

9. Throughout my career, I have also been continuously involved in the specification design, layout, and evaluation of integrated circuits. For instance, at Fairchild I was responsible for the layout of several integrated circuits, including the circuit design of certain portions of those circuits. At Supertex I was responsible for the development of a family of ICs that included logic control circuitry with high voltage inputs and outputs. At both Siliconix and IXYS I had responsibility for the design and development of all of their integrated circuits.

10. Additionally, as a consultant to the semiconductor industry for the past 15 years, I have been involved in numerous circuit-related engineering projects. I have also worked on cases involving circuit patents. I have assisted clients in the development of ICs, including

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developing specifications, evaluating circuit designs and their layout, and trouble-shooting circuits to increase yield.[1]

II. Technology Background

A. Semiconductor Manufacturing Process and Process Technology

11. Semiconductor device fabrication is the process used to create the integrated circuits or "chips" that are present in everyday electrical and electronic devices. It is a multiple-step sequence of photographic and chemical processing steps during which electronic circuits are gradually created on a wafer usually made of pure semiconducting material. Silicon is the most commonly used semiconductor material today.

12. The manufacturing process can be broken down into three major steps (1) Front End Processing, (2) Wafer sort, and (3) Device Packaging and Test..

13. Front End Processing : "Front End Processing" refers to the formation of the transistors directly on the silicon or "silicon on insulator. In memory devices the individual memory cells are also fabricated at this time. Once the various semiconductor devices have been created they are then interconnected to form the desired electrical circuits. The resulting wafer consists of hundreds, if not thousands, of dice (individual electronic devices) that perform a specific electronic function. This suit focuses on flash memory devices.

14. Wafer Sort and Test: Once the Front End Process has been completed, the semiconductor devices are subjected to a variety of electrical tests to determine if they function properly. The Automated Test Equipment ("ATE") used to perform the electrical testing of Flash Memory wafers is the focus of this lawsuit.

15. Device Packaging and Test: Once tested, the wafer is then broken into individual dice (die singulation). Only the good dice go on to be packaged. Plastic or ceramic packaging involves mounting the die, connecting the die pads to the pins on the package, and sealing the die. Tiny wires are used to connect pads to the pins. The packaged chips are retested to ensure that they

1. The Silicon Valley Expert Witness Group is being compensated for my time at my [redacted] for my work in connection with this case. This compensation is not contingent upon my performance, the outcome of this case, or any issues involved in, or related to, this case. I am also being reimbursed for authorized travel and related expenses.

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were not damaged during packaging and that the die-to-pin interconnect operation was performed correctly.

16. Testing During Wafer Sort: Flash memory wafers are tested by placing them on a memory tester. Memory testers, such as those manufactured by Verigy and Teradyne, are a piece of large electromechanical test equipment that send electrical signals to the memory device (called the Device Under Test or DUT). The electrical signals write a pattern of ones and zeros into each memory cell and then read each back to ensure that the pattern received was identical to the pattern originally written. If the pattern is not identical, the test fails and the die is marked bad.

b. Gaining Efficiency In Wafer Sort Testing

17. Memory test systems have many modules. At the highest level they consist of a memory tester, which consists of a system bay, test head, and wafer prober, The pattern of signals are programmed at the system bay, and are electrically sent through the test head. The test head interfaces to a wafer by interconnecting to a probe card. The probe card transfers the electrical signals to the wafer under test. The wafer prober holds the wafer that will be tested. It is called a touchdown when the probe card properly aligns and contacts with the wafer, and the programmed electrical signals begin to test the DUT. The fewer number of touchdowns necessary to test an entire wafer the less expensive the cost of testing the DUTS. Similarly, the greater the number of DUTS that can be tested with a single touchdown reduces the cost of test ("COT").

18. For NOR Flash Memory this write/read pattern testing must be fast and virtually flawless to ensure proper working of the DUT. NAND Flash Memory is less demanding regarding speed of the tester and the accuracy of the test.

19. As mentioned above, the greater the number of DUTS tested with a single touchdown, the less the COT. Since memory testers are large expensive machines they are sometime referred to as a "resource." In order to gain more efficiency from this "resource" circuits are put on the probe card so that the tester resource is offloaded, or "shared," so that a greater number of DUTS can be tested simultaneously. When the resource sharing is created by circuits on the probe card this is sometimes referred to as *probe card resource sharing*.

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20. In its simplest form a *probe card resource sharing* circuit consists of a circuit that simply fans out (i.e. shares) the test signal from the memory tester to two or more DUTS. This form of resource sharing is called fan out, because the signals spread out like a fan to two or more DUTS simultaneously.

21. In a more sophisticated example of *probe card resource sharing*, the probe card includes a semiconductor switch which not only fans-out, but also selectively transmits, the test signals from the memory tester to the wafer. This is commonly referred to as *multiplexing*. The switches can be implemented with electrical relays or field effect transistors ("FETS"). A multiplex circuit allows tester resources to be fanned out to multiple DUTS, while maintaining the uniqueness of each DUT, and the ability to disconnect failing DUTS.

22. *Multiplex probe card resource sharing* circuits have been and are currently being practiced by Memory manufacturers such as Micron and Intel. They have also been developed by probe card vendors such as Formfactor Inc. To the extent that probe card resource sharing circuits increase the number of DUTS simultaneously tested, it reduces the number of tester channels that memory manufacturers need to purchase from memory tester manufacturers such as Verigy and Teradyne.

c. Volatile vs. Non-Volatile Memory

23. Non-volatile memory is the general name used to describe any type of memory which does not lose its information when power is turned off. This behavior is in contrast to the most common forms of memory today – such as static random access memory (SRAM) and dynamic random access memory (DRAM) -- which both require continual power in order to maintain their data (volatile memory). Two main technologies dominate the non-volatile flash memory market today, NOR and NAND. NOR flash was first introduced by Intel in 1988. NAND flash was introduced by Toshiba in 1989.

24. Volatile Memory: SRAM and DRAM primarily differ in the lifetime of the data they store. SRAM retains its contents as long as electrical power is applied to the chip. If the power is turned off or lost temporarily, its contents will be lost forever. DRAM, on the other hand, has an extremely short data lifetime – typically a few milliseconds. This is true even when power is applied constantly. Accordingly, DRAMs must be continuously refreshed.

25. Non-Volatile Memory: As discussed in the article "Two Technologies Compared: NOR vs. NAND," (Exhibit B) two main technologies dominate the flash memory market. Though the

two technologies are similar from a fabrication perspective, these two types of flash memories have some distinct differences from a user's point of view. Table 1 highlights the major differences between NOR and NAND flash. It demonstrates the reasons why NAND flash is ideal for high capacity, low reliability, data storage (such as needed in digital cameras), while NOR flash is best used for low capacity, high reliability (such as cell phone information).

Table 1: Major Differences between NOR and NAND

	NOR	NAND
Capacity	1MegaByte – 256 MegaBytes	16Mega Bytes-2Giga Bytes
Performance	Slow erase (~600 milli sec) Fast random write (~30 micro sec) Fast random read (~8 nano sec)	Fast erase (~2 milli sec) Fast page (2048 bytes) write (~200 micro sec) Slow random read (~30 nano sec)
Access Method	Random (any memory cell at any time)	Sequential (only a block of memory cells at a time)
Reliability	Standard	Low (due to bits randomly flipping from "0" to "1")
Life Span	Les than 10% the life span of NAND	Over 10 times more than NOR
Interface	Full memory interface: apply address, receive data.	I/O only: CLE, ALE and OLE signals must be toggled.
Ease of Testing	Complicated	Simple
Ideal Usage	Highly reliable, small storage: <u>Examples:</u> Mobile Phones Set Top Boxes Home Appliances	Less reliable, mass storage only <u>Examples:</u> Digital Cameras (image storage) PC cards Compact Flash Cards MP3 players (Music storage)

26. There are many differences between NAND and NOR Flash Memory. A summary of the major differences follows:

    a. Applications: NOR is typically used where reliability is essential (such as storing a phone number in a cell phone). NAND is used were reliability it less important, but the amount of storage required is greater (such as pictures in a digital camera)

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b. Reliability & Performance: NOR offers high reliability and read performance for lower capacity applications. On the other hand, NAND offers extremely high capacity, combined with fast write and erase rates, at a lower reliability.

c. Random Access: NOR flash allows for random access to the data. In other words, the data contained at any individual memory address can be individually retrieved via a parallel interface. NAND flash does not allow for random access to data because information is retrieved in large blocks (such as 1024 to 2048 bytes) via a serial interface.

d. NOR has only one tenth ($1/10^{th}$) the lifespan of NAND Flash Memory.

27. Implications on Testing: More sophisticated testing resources are required to test NOR flash because (1) of the extremely fast read cycle, and (2) the high number of pins used to individually address each memory storage cell. The read cycle time of less than 8 nanoseconds for NOR memory forces testing equipment to operate with extremely short time cycles. For example, Flash Enhancer operates on a 5 nanosecond cycle time (12 nanosecond accounting for skew) to ensure proper testing of a NOR memory device. Since each NOR memory cell is individually readable the device must have 32 or 64 pins dedicated to addressing. In contrast, NAND memories require only 8 pins to read the memory cells. This four or eight time increase in the number of address pins requires tester equipment with four to eight times the number of channels to test the device.

d. Equipment Used in Memory Testing – Automated Test Equipment ("ATE")

i. Overview

28. This overview of ATE liberally quotes and paraphrases from US Patent 6,366,112. Numbers are included for references in the diagrams taken straight from the patent. A true and correct copy of the US 6,366,112 is included in Exhibit C.

29. As discussed in US 6,366,112 semiconductor wafers are tested prior to separation [sawing of the wafer, which contains hundreds of die] into individual die, to determine the electrical

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characteristics of the integrated circuit contained on each die. A typical wafer level test system includes a tester for generating test signals 26, a wafer prober for handling and positioning the wafers 18, 24, a probe card 20 for making temporary electrical connections with the wafer 10 , and a prober interface board 28 to route signals from the tester pin electronics to the probe card. Such a system is diagramed below in Figure 3 from the '112 patent.

(PRIOR ART)

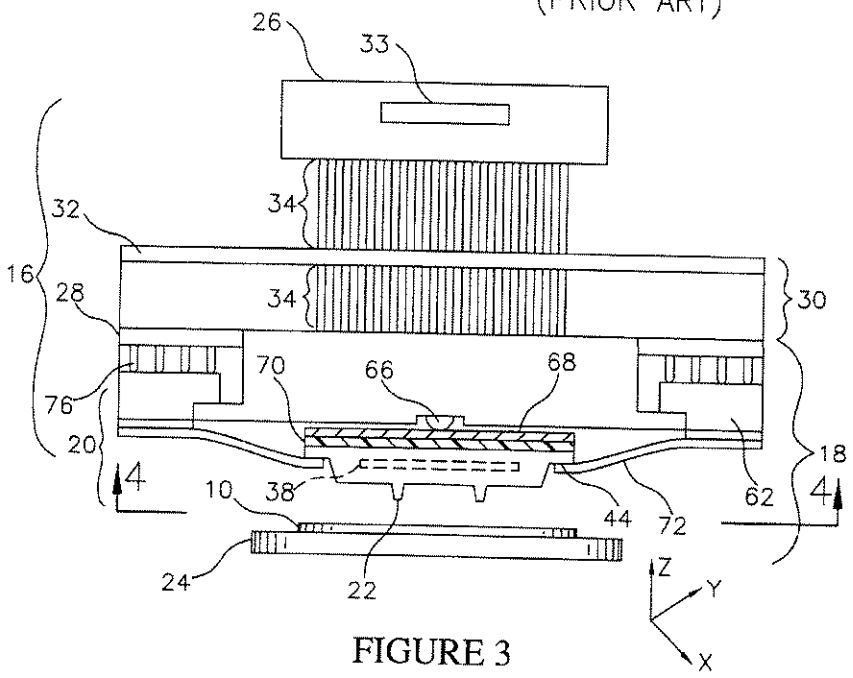

FIGURE 3

30. The test signals can include specific combinations of voltages and currents transmitted through the pin electronics channels of the tester to the probe interface board, to the probe card, and then to one or more devices under test ["DUT"] on the wafer. During the test procedure response signals such as voltage, current and frequency can be analyzed and compared by the tester to required values. The integrated circuits that do not meet specification can be marked or can be mapped using software. Following testing, some defective circuits can be repaired by actuating fuses to inactive the defective circuitry or substitute redundant circuitry.

31. Different types of probe cards have been developed for probe testing semiconductor wafers. The most common type of probe card includes elongated needle probes configured to

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electrically engage die contacts, such as bond pads, or other contacts on the wafer. Figures 6 and 7 of US 4,563,640 (Exhibit D) shown the bottom and cross section of a probe card with fixed probes. Although widely used, needle probe cards are difficult to maintain and unsuitable for high parallelism applications, where multiple dice must be tested at the same time. Long needles can also generate parasitic signals at high speeds (e.g. >500MHz).

32. Due to these disadvantages other forms of probe cards have been developed such as buckle beam probe cards [as described in U.S. Pat. No. 4,027,935 – a copy is attached as Exhibit E], membrane probe cards [as described in U.S. Pat. No 4,918,383 – a copy is attached as Exhibit E]. Both of these types of probe cards have disadvantages of their own, most notably, that maintaining electrical contact between a large number of die and a the probe card is extremely difficult.

33. It is desirable and advantageous to functionally test each die at the wafer level, often at more than one temperature. Full functionality testing of each die requires a large number of connections with each die, and separate input/output paths between each die and the tester. Parallel input/output paths are required between the tester and multiple locations on the die. The number of drive only and input/output channels is fixed for a particular tester by its manufacturer. Purchasing the additional parallel tester channels necessary to test an entire wafer of die in parallel can be exorbitantly expensive. Therefore, a solution that can share resources between the tester channels and the DUT is cost effective.

ii. Resource Sharing (Multiplexing)

34. The concept of "resource sharing" has been known in the industry for approximately twenty years. Generally, it refers to electronic circuitry attached to the probe card that allows existing tester channels to drive/receive signals from multiple DUTS by multiplexing the signals. Multiplexing including "fan out" or selective transmission of tester signals to the DUT. The

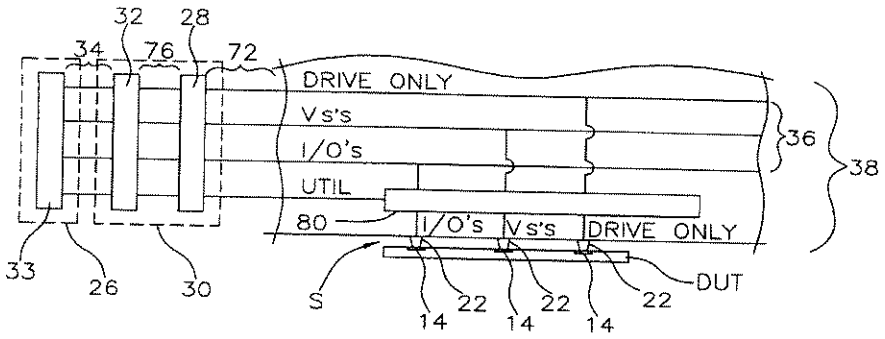

FIGURE 8A

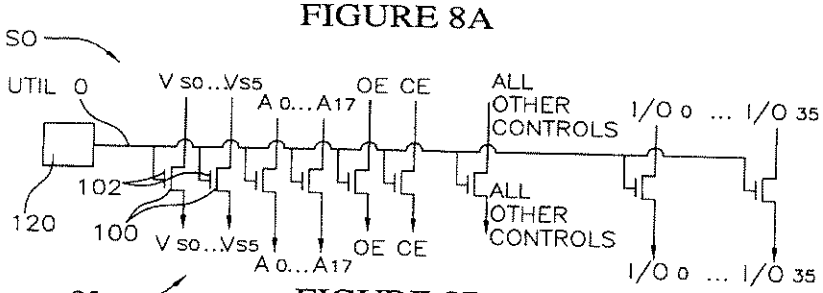

FIGURE 8B

multiplex circuit can include active electrical switch devices, such as field effect transistors (FETS), or even application specific integrated circuits (ASIC). Figures 8A and 8B from the '112 patent are diagrams of one such board.

35. The multiplex circuitry allows tester resources to be fanned out to multiple devices under test, while maintaining the uniqueness of each device, and providing the ability to disconnect failing devices. The additional control of the test signals also speeds up the testing process, and allows higher wafer throughputs using he same tester resources. Fan out allows one tester channel to simultaneously drive pads on two DUTs. This capability saves the cost of one tester channel.

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36. The probe card and its contacts can be configured to electrically engage one die at a time, or multiple die at the same time, up to all of the dice contained on the wafer. In addition, each probe card contact can be enabled or disabled as requested by the multiplexer circuit, to selectively write (send) the test signals to the die contacts, and to selectively read (receive) output signals from the die contacts. Multiple die can be written to in parallel by multiplexing

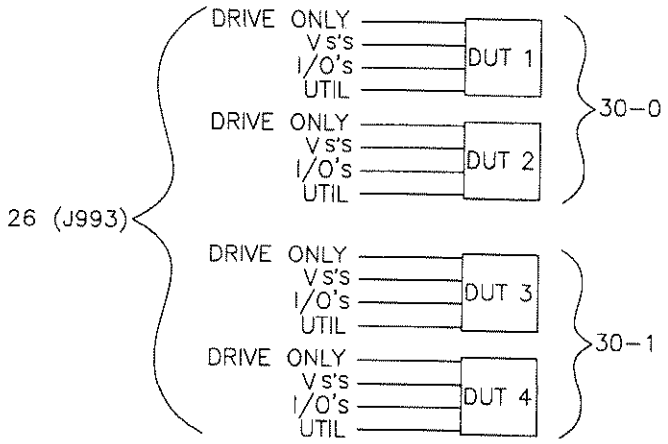

FIGURE 8C
(PRIOR ART)

the drive only and the I/O resources of the tester. Following the write step, multiple die can be read in parallel. Figure 8C from the '112 patent shows how a tester without a resource sharing probe card tests DUTS.

37. Figure 8D from the '112 patent diagrams how a multiplex circuit reduces the number of tester channels needed by sharing tester channels across multiple DUTS.

iii. <u>The Specific Problem of Testing Memory</u>

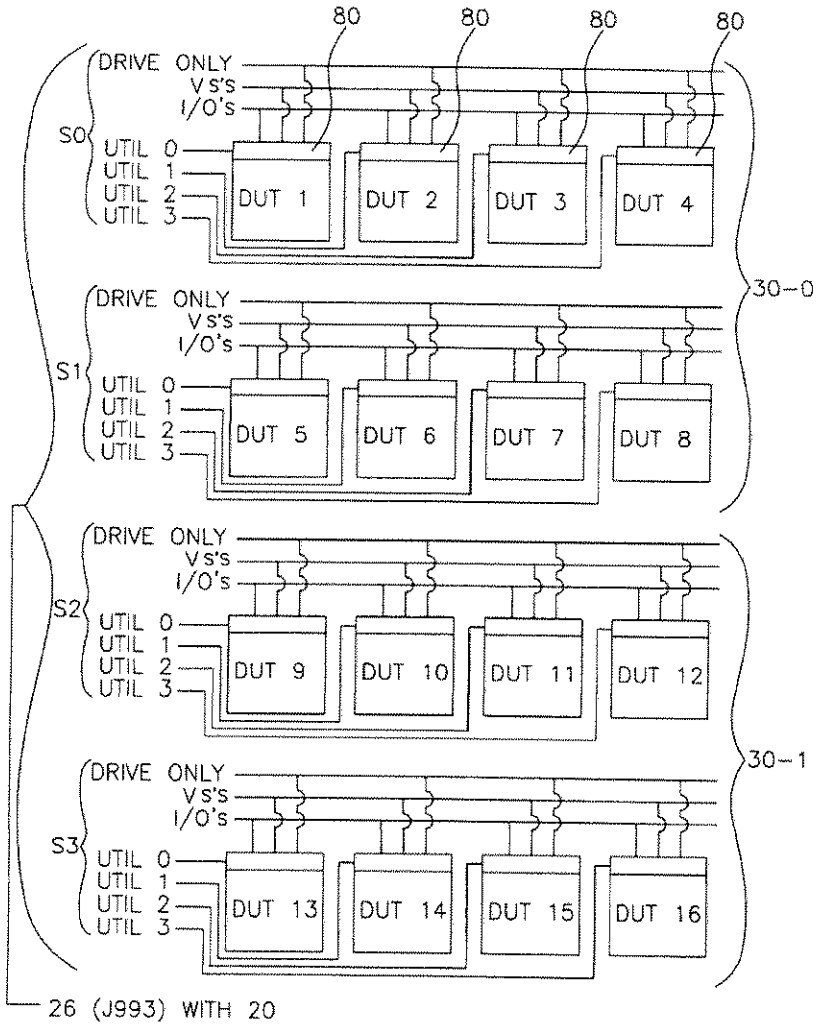

FIGURE 8D

38. This discussion concerning the specific problems of testing memory devices liberally quotes and paraphrases from PG Pub US 2005/0237073. Numbers are included for referencing the diagram that is taken straight from the patent. A true and correct copy of the PG Pub US 2005/0237073 is included in Exhibit G.

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39. PG Pub US 2005/0237073, dated October 27, 2005 describes selective multiplexing circuitry for testing memory devices in great detail. It describes such circuitry as "enabling fan out of a test channel signal to multiple DUTs..."

40. The increasing density and complexity of modern memory devices has meant longer test times per device and low test throughput rates. Combating the increasing testing times has typically involved increasing the number of devices being tested in parallel. Unfortunately, efficiencies in testing memory have not cost effectively kept pace with the rate of increasing density of semiconductor memory. Increasing the number of devices tested in parallel has meant increased pin counts and complexity of memory testers and probe cards. In other words, as the density of memory doubles every 12-18 months, the effort required to test the devices has doubled as well. This increasing density has created a business situation where it may cost more to test a semiconductor chip than it does to manufacture it!

41. Memory testing requires the tester to provide address signals, control signals for commands, power supply, and input/output (I/O) signals. Testing focuses on writing and reading from the memory. The write operation may be performed by first selecting an address location of the write operation by asserting the address along the address lines. The data to be written may then be provided along the data lines to write the data in the selected address location. Thereafter, a read operation may be performed at the address where the write was performed to verify that the data retrieved is indeed the data that was written. To perform the read operation, the address may be asserted again along the address lines and the data on the data lines may be capture. The control signals may be used to indicate the type of command being executed to facilitate communication between devices.

42. One solution to reducing total testing time and improving throughput is to simultaneously test multiple memory devices in parallel. Such a system is diagrammed below in Figure 6 from US Patent Application 2005/0237073.

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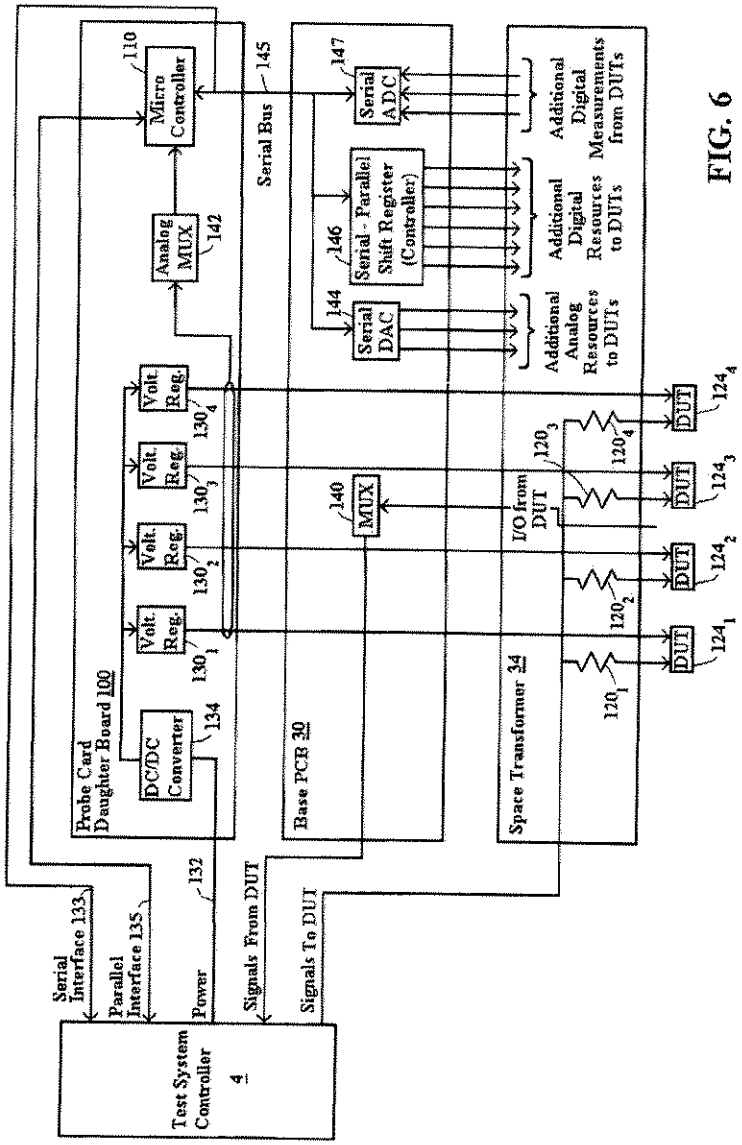

FIG. 6

43. Memory testing may comprise providing address signal, control signals for commands, power supply, and input/output (I/O) signals. Testing, for example, may involve performing a write in operation followed by a read operation. The distribution of signals to multiple DUTs is described as shown below in one embodiment of US 2007/0237073.

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44. The serial interface bus is provided between the daughter card (and other daughter cards if used) and base PCB. The serial bus enables communication between the base PCB and daughter cards with a minimum number of connector and wiring resources. The serial to parallel converter, such as serial-parallel shift register is provided on the base PCB for distributing the serial bus signals to individual DUTs internal to the PCB with a minimum amount of routing lines and connector resources.

45. Figure 2A of US patent application 2007/0165469 (11/333,037) (a true and correct copy is

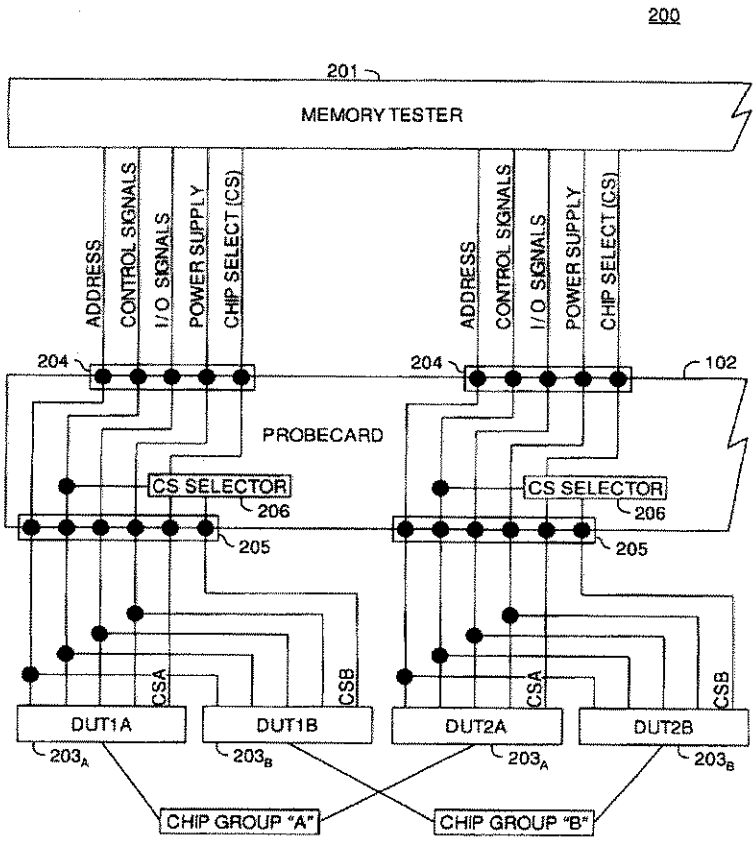

FIG. 2A

attached as Exhibit O) diagrams an embodiment of the "selective transmission" approach discussed in the '112 patent mentioned above.

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46. The ''037 patent application described the embodiment as follows: [This is a verbatim quote.]

> [0020] FIG. 2 illustrates an exemplary test system 200 according to one embodiment of the invention. System 200 comprises a memory tester 201, probe card 202 and a plurality of DUTs 203. A plurality of sets of test signals 106 couple the memory tester 201 to a respective set of input ports 204 of probe card 202, as illustrated. Four such input ports 204 are shown. Each set of input ports may comprise ports to receive address, control, I/O, power and chip select signals. While address, control, I/O, power and chip select signal ports are illustrated, one skilled in the art will recognize that any combination of the above mentioned signals or any additional signal ports may be utilized for performing the necessary testing operations.

III. Analysis

A. Probe Card Resource Sharing is Public & Well Known in the Semiconductor Test Industry

47. Multiplexing (whether by fanning out or switching) on probe cards is well known in the industry as demonstrated by the US Patent disclosures outlined above ("the Disclosures"). One embodiment of US 6,366,112 discusses actual channel connections and the physical quantities (current, voltage) that may be provided to a device under test, and the quantities (current, voltage, resistance) that may be measured.

48. Most notably the '112 patent specifically discusses an illustrative embodiment of how the multiplexing probe card is connected to either a Teradyne J993 tester or a J994 tester. It discloses a 1:N multiplexing scheme and illustrates specifically a 1:4 multiplexing scheme. The patent has been assigned to Micron, a NAND memory manufacturer.

49. Equally notable, but not used above for the technology discussion, are the following patents published prior to any work on the [redacted]

    a. Additional Micron Patents US 6,300,786 (Oct 9, 2001) and US 6,246,250 (June 12, 2001). The patents disclose the same or similar content as the '112 patent discussed in detail above. Both patents disclose and claim additional inventions and methods for resource sharing probe cards with on-board multiplex circuitry. These patents are attached in Exhibit PP.

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b. Samsung Electronics Co., Ltd Patent US 6,888,366 B2 (May 3, 2005) which discloses both a semiconductor test system and test method for writing to and reading from memory similar to the application of the multiplexing concepts at issue here. This patent is attached in Exhibit PP.

c. Three patents assigned to FormFactor, Inc. of Livermore, CA, a resource sharing probe card manufacturer; US 6,798,225 B2 (September 28, 2004), US 6,678,850 B2 (January 13, 2004), and US 6,784,674 (August 31, 2004). These three patents all disclose and claim inventions related to multiplexing on probe cards and fan out of signals on probe cards so that multiple DUTS can be tested simultaneously. These patents are attached in Exhibit PP.

50. From review of these patents, patent applications, and my own knowledge of semiconductor test, I conclude that Field Effect Transistors ("FETs") or other semiconductor switches mounted on probe cards for use in sharing testing resources was public and well known in the industry at the time the [redacted].

B. STS Flash Enhancer is Not Functionally Similar to or Derived From Verigy's [redacted] Chip

51. This analysis is being done because the Leventhal Declaration asserts that Flash Enhancer appears to perform the same functions as Verigy's . . [redacted].[2]

52. Before beginning this analysis it is important to note that the [redacted] Matrix ASIC is publicly discussed in detail in the September 2005 lead article of Evaluation Engineering magazine. A copy of the article is attached as Exhibit QQ. The [redacted] code name is explicitly used, and the article describes a 1:4 switch matrix [redacted] Figure 3 in the article is a detailed diagram of the ASIC.

[2] Exhibit I: Leventhal Declaration ¶21.

53. A copy of Figure 3 from the article is shown here for

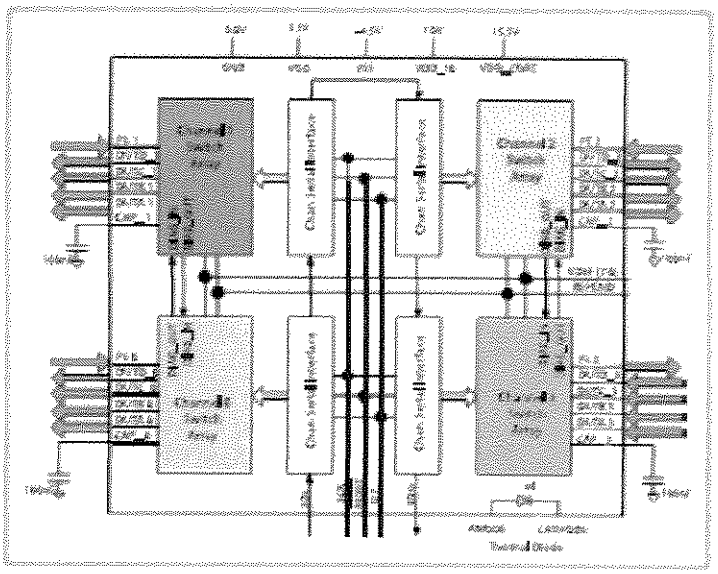

Figure 3. The Kiowa Switching ASIC

clarity.

54. A true and correct copy of the [redacted] is attached as Exhibit FF. In comparing this specification with the Flash Enahancer data sheet I conclude that the [redacted]

a. [redacted]

b. [redacted]

c. [redacted]

d. [redacted]

e. [redacted]

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55. In addition there exist differences in the overall frequency of operation and power required to drive the ASICs, the density of circuits, and how each handles automated test pattern generation.

C. The Information Contained in the Pochowski Exhibits is Publicly Available, Well Known in the Industry, or Not Used in the Existing Flash Enhancer Product

[redacted]

56. The [redacted] 6 from Exhibit A of the Pochowski declaration includes the following:

a. [redacted]

57. The RFQ conceptually specifies a [redacted] Multiple vendors manufacture SP4T switches (see data sheets of Exhibit X). If any engineer was presented with a problem that required [redacted] switches but had limited space, a well known solution is to consolidate all sixteen into a single package either through fabrication or by placing sixteen individual die into a multi-chip module ("MCM").

58. One vendor that manufactures a SP4T switch is Honeywell. The HRF-SW1020 RF switch is a single SP4T switch. [redacted].

59. This type of switch technology is well known in the industry. Data sheets from other companies that discuss similar switch technology are listed below.

a. Peregrine SP4T, SP7T (true and correct copy attached as Exhibit L)
b. Hetlite SP4T (true and correct copy attached as Exhibit M)
c. RFMD SP4T (true and correct copy attached as Exhibit N)
d. Skyworks SP4T (true and correct copy attached as Exhibit O)
e. Tyco SP4T (true and correct copy attached as Exhibit P)

[redacted]

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